REMARKS

In the Office Action of September 14, 2004, claims 1, 8, 11, 17 to 27 and 34 have been rejected and objections were lodged against claims 8 to 10, 12 to 16 and 28 to 33. Herein, claims 8, 10, 12-16 and 28-33 are amended and claims 35-46 are added. No claims are canceled. Reconsideration is requested.

Claim Objections

With respect to claims 8 and 9, an objection was made that the claims, which had depended from claim 1, recite "each clear code register..." whereas claim 1 recites a single clear code register. In response, claims 8 and 9 have been amended to depend from claim 5 instead of claim 1.

With respect to claim 10, an objection was made that the claim recites "...a DAC register...to each DAC..." where as claim 1, from which it depends, recites only a single DAC. In response, claim 10 has been amended to depend from claim 2 instead of claim 1.

With respect to claims 10-12, an objection was made that these claims recite "...the clear code stored in each clear code register..." whereas claim 1 does not clearly recite more than one clear code register. In response, claims 12-16 are amended to depend from claim 5, instead of claim 1.

With respect to claims 28-32, an objection was made that such claims recite "...each clear code register is selected...and that this leads to a similar lack of clarity." In response, claims 28-32 are amended to depend from claim 23, instead of claim 19.

With respect to claim 33, an objection was made that the claim recites "...a DAC register is provided...to each DAC..." whereas there is no clear indication in claim 19, from which it depends, that more than one DAC is included. Accordingly, the dependency of claim 33 has been amended so that claim 33 now depends from claim 21, instead of claim 19.

Accordingly, all objections are now resolved and claims 8-10, 12-16 and 28-33 should be allowed.

New Claims

Because of the revisions which have been made to claims 8 to 10 and 12 to 16, new claims 36 to 41, which are of substantially similar scope to the corresponding revised claims, but which are correctly dependent on claim 1, have been added. New claims 42 to 46, which are of substantially similar scope to the corresponding revised claims 28 to 33, but which are correctly dependent on claim 19, have also been added.

Claim Rejections - 35 USC §102

Claims 1, 8, 11, 19-20, 27 and 34 have been rejected under 35 USC §102(e) as anticipated by Russell, U.S. Patent 6,392,578.

Starting with claim 1, reconsideration is requested. The rejection of claim 1 is incorrectly made, and is unjustified. The invention of claim 1 is novel.

Claim 1 is directed towards an integrated circuit having the following limitations:

(a) a digital-to-analog converter (DAC),

(b) a clear code register for storing a digital clear code, and

(c) a control circuit responsive to a clear code signal for transferring the clear code from the clear code register to the DAC, so that the DAC outputs an analog output signal corresponding to the clear code in the clear code condition.

Contrary to the Office Action, Russell does not show an integrated circuit which comprises features (a) to (c) as set out above.

Manifestly, the Examiner has misinterpreted the Russell disclosure. Russell shows a DAC which includes a register 7 for storing a transfer coefficient of the DAC. The transfer coefficient is obtained from the formula which is set forth in column 4, lines 32 and 33 as being the predetermined ideal value of the analog output divided by the actual value of the analog output. In use, the digital codes applied to the input of Russell's DAC are multiplied by the transfer coefficient stored in the register 7, for correcting for inaccuracies in the DAC. Nowhere does Russell disclose an integrated circuit comprising a DAC which includes a clear code register and a control circuit which is responsive to a clear signal for transferring the clear code from the clear code register to the DAC. Furthermore, there is no suggestion in Russell that the transfer coefficient in the register 7 could be transferred to the DAC in response to a clear code

signal. In fact, quite the contrary is the case, since the transfer function of Russell is used for multiplying codes applied to the input of the DAC. Thus, the transfer coefficient of Russell is *never* transferred to the DAC. Consequently, Russell does not anticipate the invention of claim 1.

The rejection of claim 8 is mooted by the amendment of claim 8 to depend from claim 5, inasmuch as claim 5 has not been rejected as anticipated by Russell.

Claim 11 depends directly from claim 1 and is novel for the same reasons as applied to claim 1. Claim 19 is a method claim that parallels apparatus claim 1. Accordingly, claims 19, 20, 27 and 34 novel over Russell for the same reasons already given, as well as any additional reasons which may pertain due to the further limitations of these claims.

Claims 17-18 have been rejected under 35 USC §102(e), also, as anticipated by Tabler, U.S. Patent 6,466,149. Tabler discloses a segmented digital-to-analog converter for processing an N-bit input digital signal. A first segment of the converter processes the two most significant bits of the digital signal, and a subsequent segment of the converter processes the least significant bits of the digital signal. The Examiner in particular refers to Fig. 4 of Tabler. Fig. 4 discloses a dual 10-bit DAC which comprises two segments, namely, a top 10-bit DAC 30, and a bottom 10-bit DAC 34. An interface and control logic circuit 20 receives the input digital signals for initial processing, and a configuration register 32. 10-bit volatile control registers 26 and 28 are provided for holding the current digital value being converted by the corresponding DAC 30 and 34. 10-bit non-volatile registers 22 and 24 are also provided for each DAC 30 and 34 for holding a value that can be recalled whenever the device is powered on, based on the setting of the configuration register 32.

The 10-bit volatile registers 26 and 28 of the respective DACs 30 and 34 can be set to any value by the serial interface and control logic 20. Examples of values to which the volatile control registers 26 and 28 can be set are a zero-scale value, a mid-scale value or a full-scale value, or the pre-set value stored in the corresponding non-volatile register 22 or 24.

However, Tabler fails to disclose the provision of a clear code register for storing a digital clear code. Furthermore, Tabler fails to disclose a control circuit which is responsive to a clear signal for transferring the clear code from such a clear code register to the DAC, so that the DAC outputs an analog output signal corresponding to the clear code in the clear condition.

Even if the non-volatile registers 22 and 24 of Tabler were considered to be capable of storing a digital clear code, which the Applicant does not concede, there is no disclosure, nor is there any suggestion that such a code would or could be transferred from either of the non-volatile registers 22 and 24 to the corresponding DAC in response to a clear signal.

Claim 17 is directed towards a multi-channel integrated circuit, which comprises a plurality of channels, and each channel is provided with a DAC. The multi-channel integrated circuit of claim 17 also requires a plurality of clear code registers, which are similar to that claimed in claim 1, and a control circuit, which is likewise similar to that claimed in claim 1. Accordingly, claim 17 is of slightly narrower scope than claim 1, and should likewise be allowable. Claim 18 is dependent on claim 17.

Accordingly, Tabler fails to disclose the invention of claims 17 and 18.

Claim Rejections - 35 USC §103

Claims 21-26 have been rejected under 35 USC §103(a) as unpatentable over Russell in view of the Applicant's admitted prior art. However, the rejection is in error. It starts from the erroneous premise that "Russell discloses every aspect of the claimed invention (see the above rejected claims) except for the multi-channels aspect." This initial premise is factually erroneous, as explained above. Russell lacks far more than simply the multi-channels aspect. As stated above, claim 19 is directed towards a method which substantially corresponds to the features claimed in respect of the integrated circuit of claim 1. Accordingly, the argument submitted above with respect to claim 1 applies also with respect to claim 19. Thus, Russell lacks, among other things, a disclosure of a DAC which includes a clear code register in the integrated circuit, storing a clear code in the clear code register and transferring a clear code from the clear code register to the DAC in response to a clear signal. The assertedly admitted prior art also fails to show this combination of limitations. Accordingly, there is no way to combine Russell and such art to arrive at the claimed invention, whether or not there can be found a proper motivation to suggest such a combination (which is not conceded). The subject matter of claims 21-26 therefore is not obvious over any combination of references of record, including the allegedly admitted prior art. The rejection thus should be withdrawn.

For the foregoing reasons, the Application will be seen to now be in order for allowance, and a Notice of Allowance is respectfully requested.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

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